WHAT IS CLAIMED IS:

1. A circuit that generates a synchronous signal used in a pulse width modulation (PWM) signal generation, comprising:

a feedback loop for generating an error-amplified voltage; and

a synchronous signal generator coupled to said feedback loop for receiving said error-amplified voltage and being controlled by said error-amplified voltage to generate said synchronous signal,

wherein said synchronous signal generator comprises a voltage-controlled oscillator (VCO) for generating said synchronous signal.

2. The circuit according to claim 1, wherein said synchronous signal generator further selectively comprises a pulse generator coupled to said VCO to generate said synchronous signal.

3. The circuit according to claim 1, wherein said circuit further comprises a PWM comparator coupled to said synchronous signal generator for receiving said synchronous signal to generate a PWM signal.

4. The circuit according to claim 3, wherein said PWM comparator comprises:

a comparator coupled its inverting input to said error-amplified voltage and its noninverting input to aa ramp signal for comparing said error-amplified voltage with said ramp signal to produce a comparison output; and

a flip-flop circuit coupled to said comparison output and said synchronous signal for generating said PWM signal.

5. A circuit that generates a ramp signal used in a pulse width modulation (PWM) signal generation, comprising:

a feedback loop for generating an error-amplified voltage; and

a ramp generator coupled to said feedback loop for receiving said error-amplified voltage and being controlled by said error-amplified voltage to generate said ramp signal,

wherein said ramp generator comprises:

a timing capacitor to be charged and discharged for generating said ramp signal;

a charge current source in which its magnitude is controlled by said error-amplified voltage so as to charge said timing capacitor and generate a rising slope of said ramp signal; and

a discharge current source in which its magnitude is controlled by said error-amplified voltage so as to discharge said timing capacitor and generate a descending slope of said ramp signal.

6. The circuit according to claim 5, wherein said circuit further comprises a PWM comparator coupled to said ramp generator for receiving said ramp signal to generate said PWM signal.

7. The circuit according to claim 6, wherein said PWM signal is selectively input to said ramp generator with said error-amplified voltage so as to generate said ramp signal.

8. The circuit according to claim 6, wherein said PWM comparator comprises:

a first comparator coupled its inverting input to said ramp signal and its noninverting input to a high level reference voltage for comparing said ramp signal with said high level reference voltage to produce a first comparison output;

a second comparator coupled its noninverting input to said ramp signal and its inverting input to a low level reference voltage for comparing

said ramp signal with said low level reference voltage to produce a second comparison output; and

a flip-flop circuit coupled to an output of said first and second comparators for generating said PWM signal.

9. The circuit according to claim 6, wherein said PWM comparator is a hysteretic comparator.

10. A synchronous signal generation method used in a pulse width modulation (PWM) signal generation employing a circuit comprising a feedback loop and a synchronous signal generator having a voltage-controlled oscillator (VCO) coupled to said feedback loop for generating said synchronous signal, comprising steps of:

generating an error-amplified voltage from said feedback loop; receiving said error-amplified voltage by said synchronous signal generator; and

controlling said synchronous signal generator by said error-amplified voltage so as to generate said synchronous signal.

11. The method according to claim 10, wherein said synchronous signal generator further selectively comprises a pulse generator coupled to said VCO to generate said synchronous signal.

12. The method according to claim 10, wherein said circuit further comprises a PWM comparator coupled to said synchronous signal generator for receiving said synchronous signal to generate a PWM signal.

13. The method according to claim 12, wherein said PWM comparator comprises:

a comparator coupled its inverting input to said error-amplified voltage and its noninverting input to a ramp signal for comparing said

error-amplified voltage with said ramp signal to produce a comparison output; and

a flip-flop circuit coupled to said comparison output and said synchronous signal for generating said PWM signal.

14. A ramp signal generation method used in a pulse width modulation (PWM) signal generation employing a circuit comprising a feedback loop and a ramp generator with a charge current source, a timing capacitor and a discharge current source, comprising steps of:

generating an error-amplified voltage from said feedback loop;

controlling said charge current source to charge said timing capacitor and generate a rising slope of said ramp signal in which said charge current source's magnitude is controlled by said error-amplified voltage and said charge current source's power on state is controlled by a high level of a PWM signal; and

controlling said discharge current source to discharge said timing capacitor and generate a descending slope of said ramp signal in which said discharge current source's magnitude is controlled by said error-amplified voltage and said discharge current source's power on state is controlled by a low level of said PWM signal.

15. The method according to claim 14, wherein said ramp generator is coupled to said feedback loop for receiving said error-amplified voltage and being controlled by said error-amplified voltage to generate said ramp signal.

16. The method according to claim 14 wherein said circuit further comprises a PWM comparator coupled to said ramp generator for receiving said ramp signal to generate said PWM signal.

17.The method according to claim 16, wherein said PWM signal is selectively input to said ramp generator with said error-amplified voltage so as to generate said ramp signal.

18.The method according to claim 16, wherein said PWM comparator comprises:

a first comparator coupled its inverting input to said ramp signal and its noninverting input to a high level reference voltage for comparing said ramp signal with said high level reference voltage to produce a first comparison output;

a second comparator coupled its noninverting input to said ramp signal and its inverting input to a low level reference voltage for comparing said ramp signal with said low level reference voltage to produce a second comparison output; and

a flip-flop circuit coupled to an output of said first and second comparators for generating said PWM signal.

19.The method according to claim 16, wherein said PWM comparator is a hysteretic comparator.